DAQ system assembly and operation

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1 DAQ system overview

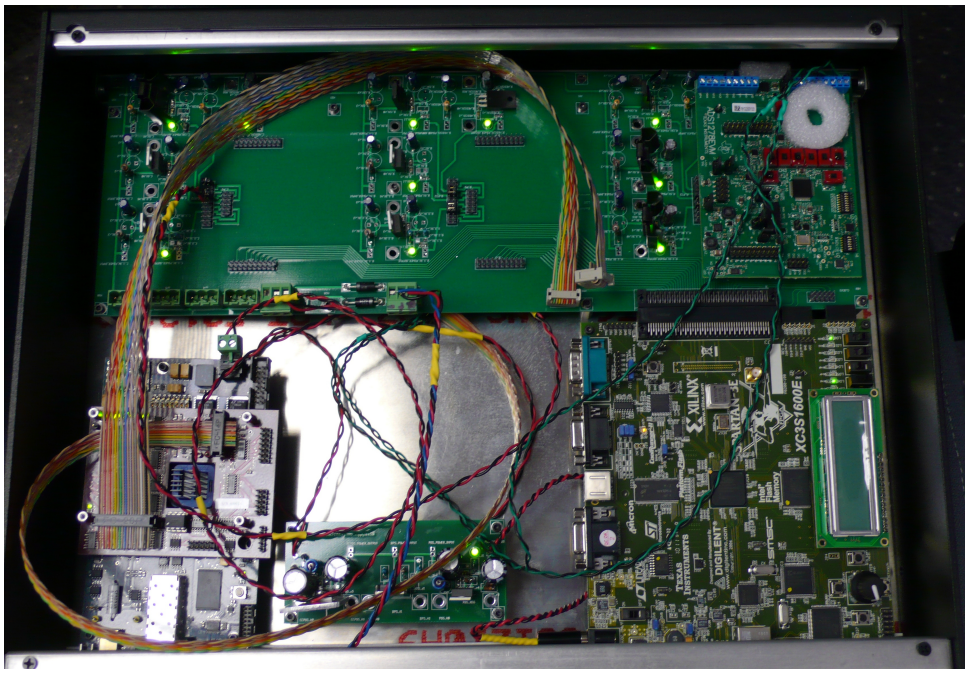

Figure 1: Assembled DAQ system

The assembled DAQ system 1 consists of FPGA board (Digilent "Spartan 3E-1600 Development Board"), FPGA power supply, custom carrier board and one or more TI evaluation modules.

At the moment the firmware supports the following TI modules:

- ADS1274EVM - 4 channel 24-bit 50kS/s ADC
- ADS1278EVM - 8 channel 24-bit 50kS/s ADC
- ADS1281EVM - 1 channel 31-bit 1kS/s ADC
- ADS1282EVM - 2 channel (via MUX, not simultaneously sampled) 31-bit 1kS/s ADC
- DAC8734EVM - 4 channel 16-bit 100kS/s DAC
- DAC1220EVM - single channel 20-bit 1000 S/s DAC

In addition the user might want to install additional custom modules (such as a timing board).

At the moment the TI modules cost $50-100, the FPGA board is $225 and the metal case is $100. Thus the largest expense for single quantity DAQ system is the PCB for the two-layer carrier board which runs around $300-$500 depending on which PCB fab you use. Thus a single system can be assembled for well under $1000 and the price comes down even more when making several units.

2 Assembly of DAQ system

2.1 Parts list

- FPGA board: Digilent "Spartan 3E-1600 Development Board"
- TI modules: `ADS1274EVM`, `ADS1278EVM`, `ADS1281EVM`, `ADS1282EVM`, `DAC8734EVM` or `DAC1220EVM`. You can also design custom module, but they will require changes in FPGA firmware.
- optional addons (e.g. timing board).
- Metal case - optional, we used Hammond Manufacturing `RMCS190313BK1`
- carrier board
- power supply board
- Voltage regulators: 5x adjustable `LM338T`, 3x +5V `LM7805`, 3x +12V `LM7812`, 3x -12V `LM7912` or equivalent parts

- Transistors: 1x `FJ4310` NPN transistor.
- Diodes: 2x of 3A or greater diodes, we used `MUR415`, 1x 1A or higher diode, we used `1N4007`, 1x 6.8V Zener diode.
- LEDs: 15x 3.5mm green LEDs
- Capacitors: 52x 0805 0.1uF surface mount, 28x through hole 10uF 25V or better.
- Resistors 0.5W or greater: 6x 47 Ohm, 6x 1 Ohm
- Voltage setting resistors for `LM338T`: 3x 240 Ohm, 3x 390 Ohm, 1x 2.7 Ohm, 1x 750 Ohm, 1x 250 Ohm. Metal film preferable.
- Misc resistors 1x 2.2 Ohm, 1x 1 kOhm, 2x 15 Ohm, 1x 180 Ohm.
- Resistors 0805 surface mount: 3x 68 Ohm, 3x 180 Ohm, 6x 560 Ohm, current limiter for diodes.
- Connectors: 1x Hirose `FX2-100` connector, 9x 2x10 0.1" header, 6x 2x5 0.1" header, 12x (or more) 0.1" jumpers, 6x 3-pin eurostyle sockets, 6x 3-pin eurostyle plugs (Phoenix contact `1755529` and `1754465`). 1x 2.1mm female plug, Digikey part number `CP3-1000-ND`.
- Hardware: 22x 3/4" standoffs (3 more for the timing board), 44x 1/4" 4-40 machine screws (6 more for the timing board).
- Template with hole layout for the bottom of the metal case.

The power sockets are convenient but optional - if needed one can solder the wires directly. The green LEDs are to make sure that none of the power supplies are overloaded due to incorrect settings (such as a short) on the modules, or larger than expected current requirements.

2.2 PCB manufacture

Our PCBs were produced from Gerber files by `http://www.custompcb.com/`. The larger carrier board has to use "PCB production" process, but can still be obtained in small quantities.

The changes to the boards or to the drill hole layout for the bottom plate should be made in Tcl description files: `carrier_board.tcl`, `power_supply.tcl` and `layout_bottom.tcl`. The files should then be converted to `PCB` layout file by running

```
./make_pcb.tcl < filename.tcl > filename.pcb
```

If any new traces were made, it is best to run design rule check. Once complete, PCB can be used to generate new Gerber files as well as PostScript output for the printer. The latter should match 1:1 to the completed board and can be used for a quick check.

2.3 Case customization

The metal case can be customized to attach individual boards to its bottom plate. An easy way to do this is by printing `layout_bottom.pdf` on a A2 paper which can then be used as a template for a metal punch.

2.4 Assembly

2.4.1 Carrier board

The two pdf files "backassembly.pdf" and "frontassembly.pdf" show board layout with necessary component outlines marked up according to their type. Connectors were marked in red, semiconductor parts in magenta, resistors in blue and capacitors in green.

The square shaped contact on all through-hole components corresponds to the negative terminal. All surface mount capacitors are 0.1uF, all through-hole electrolytic capacitors are 10uF 25V or larger. It is best to keep electrolytic capacitors under 11mm height or they will interfere with module placement.

Each module has 4 power supplies: 3.3V, +5V, +12V and -12V. Their components are marked with `*_3_3V_*`, `*_5V_*`, `*_12V_*` and `*_NEG12V_*` correspondingly.

The `*_r2` resistors serve in three roles: they drop the voltage to reduce power dissipation in voltage regulators, limit the inrush current to input capacitors and, together with input capacitors, filter out high frequency interference. Their values are 47 Ohm for 3.3 and 5V power supplies and 5 Ohm for +/- 12V power supplies.

The *_r1 surface mount resistors limit the current to the indicator LEDs. Their values are 68 Ohm for 3.3V, 180 Ohm for 5V and 560 Ohm for +/-12V power supplies.

The 3.3V power supply needs two voltage setting resistors, *_r3 (closest to the voltage regulator) is 390 Ohm, *_r4 (closest to the connectors) is 240 Ohm.

The voltage regulators should be placed with the metal side towards the flat line on the silkscreen. The -12V regulator should be bent metal side up to provide clearance for the module above.

2.4.2 Power supply

The square shaped contact on all through-hole components corresponds to the negative terminal. All surface mount capacitors are 0.1uF, all through-hole electrolytic capacitors are 10uF 25V or larger.

The resistor values are shown in table 2.

Component	Value (Ohms)	Power rating (W)
CCPOS_r2	2.2	2
CCPOS_r4	2.7	2
BPS_r1	15	2
BPS_r2	1000	0.25
BPS_r3	15	2
POS_r1	180	0.25
POS_r3	750	0.25
POS_r4	250	0.25

Figure 2: Component list for constant current power supply.

The zener diode BPS_d1 should have a threshold of 6.8V. Voltage regulators and the transistor should be placed with the heatsinks facing the line on the PCB.

2.5 Soldering

This part is mostly straightforward. Surface mount parts can be placed more easily by first adding a little solder to one pad for each part and then placing parts after melting this solder.

The headers can be held in the middle with the finger while soldering two opposite pins. It is best to check that they are straight before soldering all the other pins.

Take care when soldering FX2-100 connector J1 so that the solder does not leak through and form a bridge on the other side of the board.

The adjustable voltage regulators on the power supply board need heatsinks to function properly.

2.6 Jumper configuration

The TI modules have jumper switches that need to be configured before use. This must be done accurately to prevent damage after power up. Also the power supply to the TI modules needs to be configured as well by placing jumpers on *_PS2.

2.6.1 ADS1274EVM, ADS1278EVM

Switch bank S10 should be all HI. Switch bank S11 should be all LO except for switches S11.M1 and S11.DIV which should be HI.

Switch S1 should be set to ON BRD to use onboard reference. Amplifier switches for channels 1-8 should be set to AMP to use onboard buffer amplifiers.

Jumpers J15 and J16 should be set to EXT. Jumper J19 should be close to GPIO5. Jumper J6 should be set to FSX.

Jumper J4 should be open, jumper J17 should be closed.

The carrier board power supply jumpers should be configured as shown in figure 3.

2.6.2 ADS1281EVM, ADS1282EVM

Jumper J1 should be set to REF, jumper J2 should be set to OBCLK, jumper J3 to DVDD and jumper J10 should be set to DN (rightmost position). Jumper J7 should be all shorted, but it is ok to leave out a jumper on either AGND or DGND (but not both).

The carrier board power supply jumpers should be configured as shown in figure 4.

2.6.3 DAC8734EVM

Switches S2 and S3 should be set to 5V to use 5V reference.

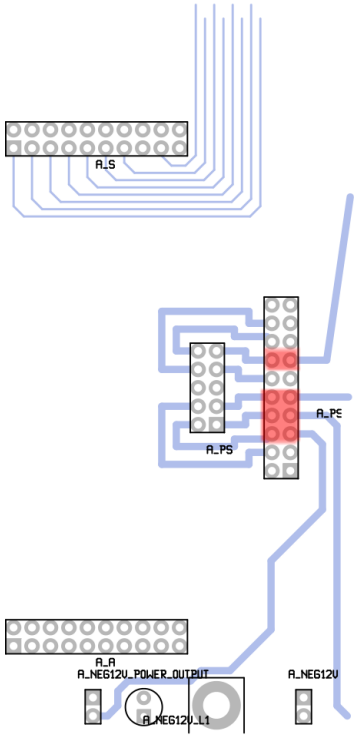

Figure 3: Carrier board jumper settings for ADS1274EVM and ADS1278EVM.

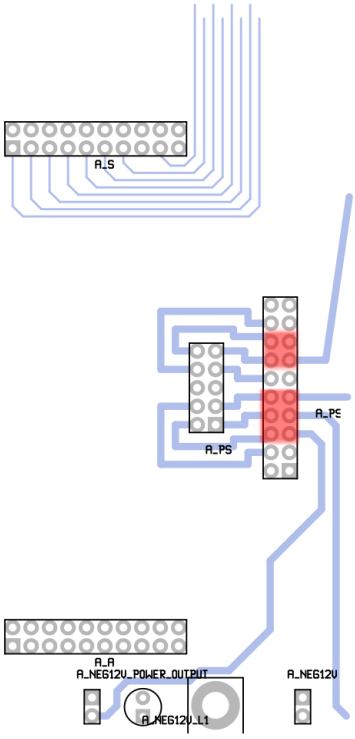

Figure 4: Carrier board jumper settings for ADS1281EVM and ADS1282EVM.

Jumpers JP6 and JP7 should be set to Ref B and Ref A corresondingly.

Jumper JP1 should be completely open.

Jumper block JP8 should have jumper installed across 1-2 pair, all other pairs should be open.

Switch bank S1 should have switches S1.1 and S1.3 low (close to mark S1) and switches S1.2 and S1.4 high.

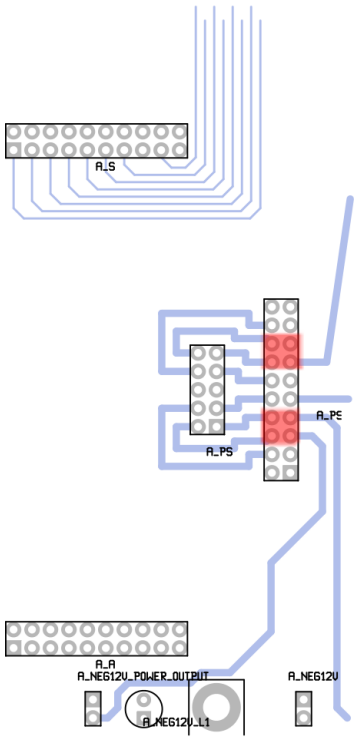

Figure 5: Carrier board jumper settings for DAC8734EVM

The carrier board power supply jumpers should be configured as shown in figure 5.

2.6.4 DAC1220EVM

Both J3 jumpers should be closed.

J5 jumper should be closed.

Switch S1 should be away from mark S1.

Switch S2 should be in the closest position to mark S2.

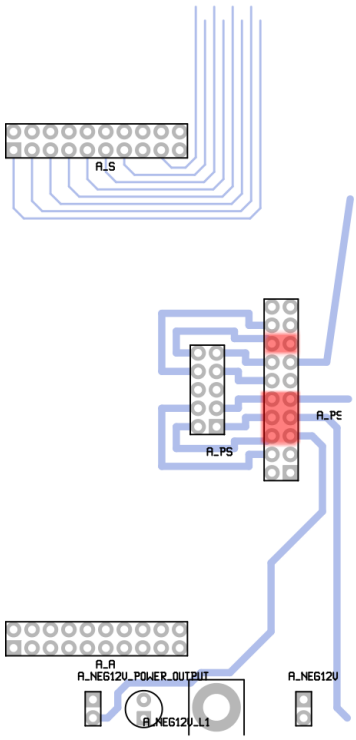

Figure 6: Carrier board jumper settings for DAC1220EVM.

The carrier board power supply jumpers should be configured as shown in figure 6.

2.7 Testing

First, apply power to carrier board alone and double check that each power supply provides the expected voltage (3.3V, 5.0V, 12V and -12V) and all the diodes light up.

Next connect power supply and check that the output is 5V and the output diode is lit.

Assemble all components into the case and apply power. Check that output of the power supply is 5V by applying probe at the FPGA input jack. Check that the internal power supply rail (`CCPOS_OUTPUT`) is below 10V. Once software is configured repeat the test to make sure that increased current from data transmission is safely handled.

3 Software setup

The FPGA board communicates with the host computer by sending Ethernet packets of type `0xda8a`. Separate boards are distinguished by MAC address. It is hardcoded into the firmware, except for bits 4 through 7 which are configured using four switches on the FPGA board.

At present two pieces of software are needed - the data acquisition daemon which runs in the background and handles traffic from the board and a Tcl/Tk GUI that displays board status and can be used to control its functions, log data, etc.

3.1 `daq_daemon`

The data acquistion daemon is a small C program that runs in the background and handles traffic to DAQ system. Each system produces 1-2 MB/s of data so a single daemon can theoretically handle up to 10 boards on a single interface. So far, we have only used one board per computer and the support for multiple boards have not been completely implemented.

The list of all configuration options can be obtained by running `daq_daemon --help`. The configuration file handles several tasks - specifies which board the daemon should communicate with, board configuration parameter, which

application specific modules should be activated. In addition it is possible to log all incoming packets into log file for debugging or acquisition of raw data. New options can be added by editing `daemon.ggo`.

```
board-mac 02:89:67:45:23:f1
daemon-mac 01:23:45:67:89:ab

jeep1-mode 1

nphases 8
sync2-divider 1023
sync2-phase 127

portA-mode 1
portB-mode 0
portC-mode 0

portA-nbits 192

sync2-config 1

reset-config 0

sampling-clock 5

data-log /dev/null
```

Figure 7: Configuration options for one ADS1278EVM board (file `config.local1`).

An example configuration file for a single ADS1278EVM board is shown on figure 7. The first two lines specify data acquisition boards MAC address and the MAC address of the host computer. The board was configured with all four switches set to 1, which is why its MAC address ends in `f1`.

The general purpose mode `jeep1` is enabled, so we can use `jeep1.tcl` user interface to connect to the board.

Sampling clock is set to 5 which indicates we are using 25 Mhz clock derived from oscillator on FPGA board. The sampling rate will be $25 \times 10^6/512 = 48828.12$ Hz.

The ADS1278EVM module has 8 24 bit channels for a total of 192 bits of data, so `portA-nbits` is configured to the value 192. If we were using ADS1274EVM we would need to set this to 96 bits instead.

```
board-mac 02:89:67:45:23:f1
daemon-mac 01:23:45:67:89:ab

nphases 8

sync1-divider 0
sync2-divider 2047
sync2-phase 4095
sync3-divider 0

portA-mode 1
portB-mode 0
portC-mode 0

portA-nbits 192

sync1-config 6
sync2-config 4
sync3-config 5
sync4-config 0

seism1-mode 1

sampling-clock 13
```

Figure 8: Configuration options for one ADS1278EVM board with timing board installed (file `config.timing1`).

Figure 8 shows similar configuration file that relies on LIGO timing board for its clock and has `seism1` software module activated (used for Homestake

DAQ system).

```
echo 33554432 > /proc/sys/net/core/rmem_default
echo 33554432 > /proc/sys/net/core/rmem_max
echo 10000 > /proc/sys/net/core/netdev_max_backlog
```

Figure 9: Linux initialization script `prepare_capture.sh`

The daq daemon uses Linux packet interface to acquire data. To insure no missed packets during heaving system activity (which, in particular, could be caused by new graphic-intensive user desktop environments) it is best to set packet capture limits to the maximum. A script to do that is shown in figure 9.

The daemon should be started with super user privileges by specifying configuration file on the command line:

```
daq_daemon --config=config.local1
```

3.2 User interface

A sample interface designed to operate with a single `ADS1278EVM` or `ADS1274EVM` module in slot `A` and `DAC8734EVM` or `DAC1220EVM` module in slot `B` can be started by running `jeep1.tcl`. Take care to always start it after `daq_daemon` is running and closing before `daq_daemon` is terminated. Otherwise a stale network connection can block `daq_daemon` from starting again for several minutes. A screenshot of the GUI in operation is shown on figure 10.

Figure 10: General purpose user interface